A Single-Phase Transformerless Inverter With Charge Pump Circuit Concept for Grid-Tied PV Applications

Jaber Fallah Ardashir, Mehran Sabahi, Seyed Hossein Hosseini, *Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, Ebrahim Babaei, *Senior Member, IEEE*, and Gevork B. Gharehpetian, *Senior Member, IEEE*

***Abstract*—This paper proposes a new single-phase transformerless photovoltaic (PV) inverter for grid-tied PV systems. The topology is derived from the concept of a charge pump circuit in order to eliminate the leakage current. It is composed of four power switches, two diodes, two capacitors, and an *LCL* output filter. The neutral of the grid is directly connected to the negative polarity of the PV panel that creates a constant common mode voltage and zero leakage current. The charge pump circuit generates the negative output voltage of the proposed inverter during the negative cycle. A proportional resonant control strategy is used to control the injected current. The main benefits of the proposed inverter are: 1) the neutral of the grid is directly connected to the negative terminal of the PV panel, so the leakage current is eliminated; 2) its compact size; 3) low cost; 4) the used dc voltage of the proposed inverter is the same as the full-bridge inverter (unlike neutral point clamped (NPC), active NPC, and half-bridge inverters); 5) flexible grounding configuration; 6) capability of reactive power flow; and 7) high efficiency. A complete description of the operating principle and analysis of the proposed inverter are presented. Experimental results are presented to confirm both the theoretical analysis and the concept of the proposed inverter. The obtained results clearly validate the performance of the proposed inverter and its practical application in grid-tied PV systems.**

***Index Terms*—Charge pump circuit, grid-tied inverter, leakage current elimination, transformerless inverter.**

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J. F. Ardashir and M. Sabahi are with the Department of Electrical Engineering, University of Tabriz, Tabriz 5166, Iran (e-mail: j.fallah@tabrizu.ac.ir; sabahi@tabrizu.ac.ir).

S. H. Hosseini and E. Babaei are with the Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666, Iran, and also with the Engineering Faculty, Near East University, 99138 Nicosia, North Cyprus, Mersin 10, Turkey (e-mail: hosseini@tabrizu.ac.ir; e-babaei@tabrizu.ac.ir).

F. Blaabjerg is with the Institute of Energy Technology, Aalborg University, DK-9220 Aalborg, Denmark (e-mail: fbl@iet.auc.dk).

G. B. Gharehpetian is with the Department of Electrical Engineering, Amirkabir University of Technology, Tehran 15875-4413, Iran (e-mail: grptian@aut.ac.ir).

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I. Introduction

OVER the last two decades, the photovoltaic (PV) power systems have become very popular among the renewable energy sources, because they generate electricity with no moving parts, operate quietly with no emissions, and require little maintenance [1], [2]. Distributed grid-connected PVs are playing an increasingly role as an integral part of the electrical grid. However, due to the large stray capacitors between the PV panels and the ground, PV systems suffer from a high common mode (CM) current, which reduces the system efficiency and may cause safety issues like electric shock. In order to eliminate the leakage currents, transformers are commonly used in the PV system to provide galvanic isolation. However, it possesses undesirable properties including large size, high cost, and weight with additional losses [3]. Thus, eliminating the transformer is a great benefit to further improve the overall system efficiency, reduce the size, and weight [4].

One of the important issues in the transformerless grid-connected PV applications is the galvanic connection of the grid and PV system, which leads to leakage current problems. For transformerless grid-connected inverters, full-bridge (FB) inverter, neutral point clamped (NPC), active NPC (ANPC) inverter [5], and many other topologies such as H5, H6, and highly efficient and reliable inverter concept (HERIC) were proposed to reduce the leakage current with disconnecting of the grid from the PV during the freewheeling modes [6]. However, these topologies are not totally free from CM current or leakage current. The leakage current still exists due to the parasitic capacitor of the switch and stray capacitance between the PV panel and ground. So, some of these topologies require two or more filter inductors to reduce the leakage current, which leads to a rise in the volume and cost of the system [7].

Fig. 1 illustrates a single-phase grid-tied transformerless inverter with CM current path, where *P* and *N* are the positive and negative terminals of the PV, respectively.

The leakage current (i_{Leakage}) flows through a parasitic capacitor (C_P) between the filters (L_1 and L_2), the inverter, grid, and ground impedance (z_g). This leakage current may cause safety problems, reduce the quality of injection current to the grid, as well as decrease the system efficiency [8]. In order to eliminate the leakage current, the CM voltage (CMV) (v_{cm})

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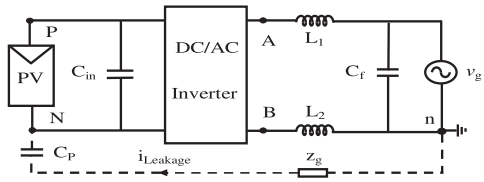

Fig. 1. Block diagram of a single-phase grid-connected transformerless inverter with a leakage current path.

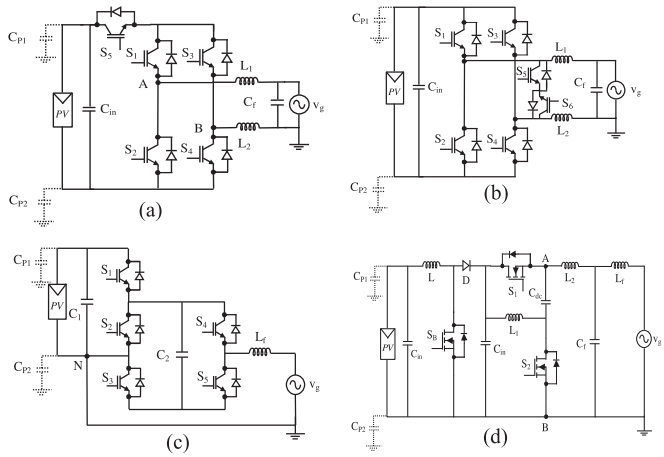

Fig. 2. Single-phase grid-tied transformerless PV inverter topologies: (a) H5 inverter, (b) HERIC inverter, (c) virtual dc-bus inverter [10], and (d) CM inverter proposed in [18].

must be kept constant during all operation modes according to [9]. The $v_{\rm cm}$ with two filter inductors (L_1, L_2) is calculated as follows:

$$v_{\rm cm} = \frac{v_{\rm An} + v_{\rm Bn}}{2} + \frac{(v_{\rm An} - v_{\rm Bn})(L_2 - L_1)}{2(L_1 + L_2)} \quad (1)$$

where $v_{\rm An}$ and $v_{\rm Bn}$ are the voltage differences between the midpoints A and B of the inverter to the dc bus minus terminal N, respectively.

If $L_1 \neq L_2$ (asymmetrical inductor), $v_{\rm cm}$ is calculated according to (1) and the leakage current appears due to a varying CMV. If $L_1 = L_2$ (symmetrical inductor), $v_{\rm cm}$ is simplified to

$$v_{\rm cm} = \frac{v_{\rm An} + v_{\rm Bn}}{2} = \text{Const.} \quad (2)$$

In this state, the CMV is constant and the leakage current is eliminated.

In some structures such as the virtual dc-bus inverter [10] and NPC inverter, one of the filter inductors is zero and only one filter inductor is used. In this state, after simplification of $v_{\rm cm}$, it will have a constant value according to (3) and the leakage current will be eliminated

$$v_{\rm cm} = \frac{v_{\rm An} + v_{\rm Bn}}{2} + \frac{v_{\rm An} - v_{\rm Bn}}{2} = \text{Const.} \quad (L_1 = 0)$$
$$v_{\rm cm} = \frac{v_{\rm An} + v_{\rm Bn}}{2} - \frac{v_{\rm An} - v_{\rm Bn}}{2} = \text{Const.} \quad (L_2 = 0). \quad (3)$$

As shown in Fig. 2, there are various transformerless grid-connected inverters based on the FB inverter in the literature to overcome these problems.

The H5 inverter that is a FB-based inverter topology, compared to the conventional FB inverter, needs one additional switch (S_5) on the dc side to decouple the dc side from the grid as shown in Fig. 2(a). This inverter has a variable CMV with a small leakage current and it suffers from low efficiency due to three switches operating at the same time [11].

As shown in Fig. 2(b), the HERIC topology needs two extra switches on the ac side to decouple the ac side from the PV module in the zero stage. HERIC combines the merits of unipolar and bipolar modulation. The main advantage of the HERIC inverter is its high efficiency due to only two switches operate at the same time in all operation modes. This topology does not allow for reactive power flow [12].

Topologies based on H6 are also proposed in [13] and [14] to eliminate the leakage current of the grid-tied PV application. These inverters consist of six power switches and some diodes for disconnecting the dc side from the grid. These topologies are more costly than the FB inverter, because they use extra switches and diodes. Another disadvantage of these topologies is lower efficiency due to the current that circulates through three power switches at the same time [15]. Several high efficient new H6 transformerless inverters are proposed in [16] and [17] to achieve lightweight and also lower cost. They have the capability of reactive power injection to the grid. The leakage current is not totally eliminated in these topologies, which is the main disadvantage of them.

Another solution to eliminate the leakage current is the direct connection of the negative PV terminal to the neutral point of the grid, such as the virtual dc-bus inverter in [10] and the unusual topology in [18]. In these topologies, the leakage current is completely eliminated by the topology structure. As shown in Fig. 2(c), the virtual dc-bus inverter is composed of five insulated-gate bipolar transistors (IGBTs), two capacitors, and one filter inductor L_f. Only one filter inductor is used in this topology to eliminate the leakage current, but it is very large. The virtual dc-bus generates the negative output voltage. The main drawback of this topology is that there is no path to charge the capacitor C_2 during the negative cycle and this will cause a high output total harmonic distortion (THD). The topology presented in [18], which is shown in Fig. 2(d), has a common ground with the grid. The number of semiconductors used in this topology is low. However, the output voltage of this inverter is only two levels including positive and negative voltages without creating the zero voltage, which requires a large output inductor L_2 and a filter. The inductor medium-type inverter [19] also called "Karschny" is another topology that is derived from the buck–boost topology. This inverter has a high reliability without capability of giving the reactive power to the grid and has four power switches in the current path at the same time, which will reduce the efficiency.

This paper introduces a new transformerless inverter based on charge pump circuit concept, which eliminates the leakage current of the grid-connected PV systems using a unipolar sinusoidal pulse width modulation (SPWM) technique. In this solution, the neutral of the grid is directly connected to the negative terminal of the charge pump circuit, so the voltage across the parasitic capacitor is connected to zero and the leakage current is eliminated. The charge pump circuit is implemented to generate negative output voltage. There is not any limitation on

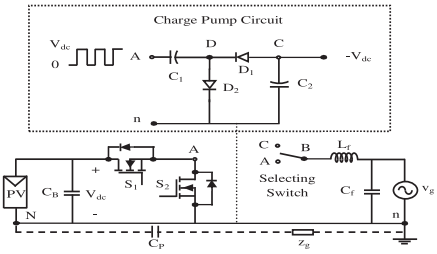

Fig. 3. Schematic diagram of the proposed inverter including the charge pump circuit.

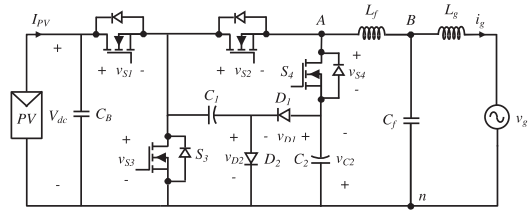

Fig. 4. Proposed single-phase transformerless grid-connected inverter.

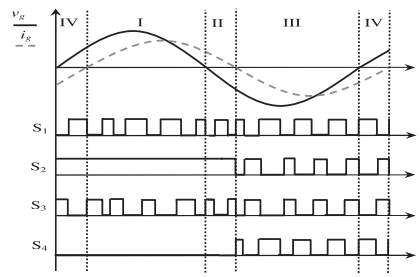

Fig. 5. Switching pattern of the proposed topology with reactive power flow.

the modulation strategy of the proposed inverter because the leakage current is eliminated by the circuit topology. The proposed topology consists of only four power switches, so the cost of the semiconductors is reduced and the power quality is improved by three-level output voltage in order to reduce the output current ripple. During operation of the proposed inverter, the current flows through two switches; thus, the conduction loss is also lower. The used dc voltage of the proposed inverter is the same as the FB inverter (unlike NPC, ANPC, and half-bridge (HB) inverters). The proposed inverter is capable of delivering reactive power into grid too. Thus, it can satisfy the requirement of the standard VDE-AR-N 4105. This paper is organized as follows. The charge pump circuit concept is explained in Section II. Based on it, a novel inverter topology is derived, and the modulation strategy and operation principles are described in detail. The current stress analysis of the switches, calculation of the power losses, and control scheme along with a comparison have been done in Section III. Experimental validations of the proposed grid-tied inverter is presented in Section IV, and finally, conclusions are given in Section V.

II. Proposed Topology and Modulation Strategy

A. Charge Pump Circuit Concept

The concept of a simple charge pump circuit to be used in the proposed topology to generate the inverter negative output voltage is shown in Fig. 3. The circuit consists of two diodes (D_1, D_2) and two capacitors (C_1, C_2). This simple charge pump circuit gives a negative dc output voltage at the point of C equal to the voltage of point A [20]. The capacitor C_1 is used to couple the voltage point of A to the node D. Two Schottky diodes D_1 and D_2 are used to pump the output voltage. When the diode D_2 is forward biased, the capacitor C_1 is charged by diode D_2. The diode D_1 is reversed in this state. When the diode D_1 conducts, capacitor C_2 is charged through the capacitor C_1 by using node n and switch S_2.

In steady state, the output voltage of the negative charge pump circuit (v_{Cn}) can be derived by

$$v_{\mathrm{Cn}} = -V_{\mathrm{dc}} + V_{\mathrm{cut-in}-D1} + V_{\mathrm{cut-in}-D2} \tag{4}$$

where V_{dc} is the input voltage, $V_{\mathrm{cut-in}-D1}$ and $V_{\mathrm{cut-in}-D2}$ are the cut-in voltages of the diodes D_1 and D_2, respectively. For high power applications, these values can be negligible.

The above principle is integrated into the proposed inverter by using additional switching devices. The voltage difference between point A of the inverter to the point n is $+V_{\mathrm{dc}}$ or zero, according to the switching state of the S_1 and S_2, respectively. The voltage of C_1 and C_2 must be kept constant during all operation modes by selecting proper switching states. Point B must be connected to the points A or C with extra switches. This creates three different voltages, namely $+V_{\mathrm{dc}}$, zero, and $-V_{\mathrm{dc}}$ for the inverter operation.

In summary, the charge pump circuit in the transformerless inverter has the following characteristics for grid-tied applications.

1) This circuit has a common line with the negative terminal of the input dc voltage and the neutral point of the grid that causes the leakage current to be eliminated.
2) The charge pump circuit has no active device and it has a lower cost for grid-tied applications.
3) The capacitor of the proposed inverter charges every switching cycle, which reduces the size of the required capacitor with the switching frequency.
4) The capacitor of the charge pump circuit charges with a switching cycle that eliminates the pulse duration sensitivity to generate the negative voltage.

B. Proposed Topology

As shown in Fig. 4, the proposed topology consists of four power switches ($S_1 - S_4$), two diodes (D_1, D_2), two capacitors (C_1, C_2) based on the charge pump circuit as described in Section II-A. An *LCL*-filter is used to eliminate harmonics of the output current. This new topology is modulated using simple SPWM. Fig. 5 shows the gate drive signals for the proposed inverter under the current lagging condition. According to the direction of the inverter output voltage and output current, the

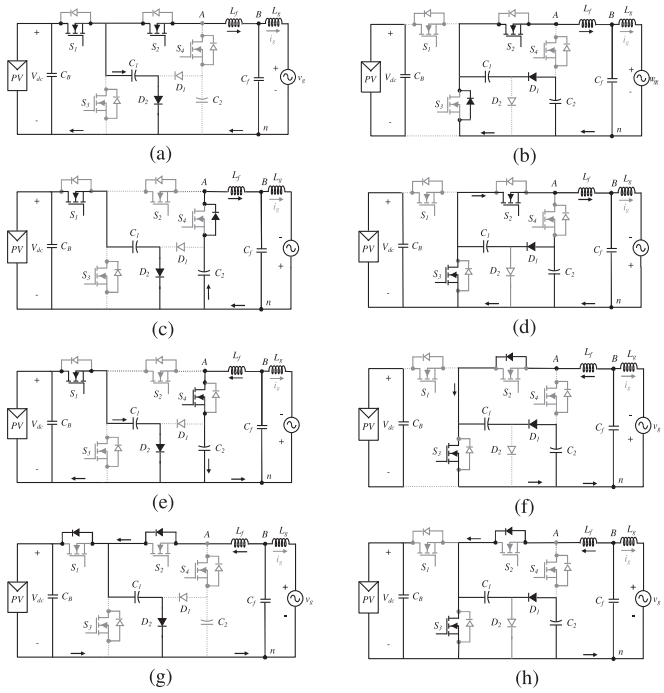

Fig. 6. Operational stages of the proposed inverter during (a), (b) region I, (c), (d) region II, (e), (f) region III, and (g), (h) region IV. (a) $v_{\mathrm{An}} = +V_{\mathrm{dc}}$, $i_g > 0$. (b) $v_{\mathrm{An}} = 0$, $i_g > 0$. (c) $v_{\mathrm{An}} = -V_{\mathrm{dc}}$, $i_g > 0$. (d) $v_{\mathrm{An}} = 0$, $i_g > 0$. (e) $v_{\mathrm{An}} = -V_{\mathrm{dc}}$, $i_g < 0$. (f) $v_{\mathrm{An}} = 0$, $i_g < 0$. (g) $v_{\mathrm{An}} = +V_{\mathrm{dc}}$, $i_g < 0$. (h) $v_{\mathrm{An}} = 0$, $i_g < 0$.

operation of the proposed inverter is divided in four regions as shown in Fig. 6. These four different regions can be defined as follows.

1) *Region I:* the inverter output voltage and the output current are positive; energy is transferred from dc side to grid side as shown in Fig. 6(a).
2) *Region II:* the inverter output voltage is negative and the output current is positive; energy is transferred from grid side to dc link as shown in Fig. 6(c).
3) *Region III:* the inverter output voltage and the output current are negative; energy is transferred from dc link to grid side as shown in Fig. 6(e).
4) *Region IV:* the inverter output voltage is positive and the output current is negative; energy is transferred from grid side to dc side as shown in Fig. 6(g).

In the regions I and IV, the switches S_1 and S_3 will be ON and OFF with the switching frequency f_s to produce positive and zero voltage while S_2 remains ON for the whole positive half-cycle. When the switches S_1 and S_2 are ON, the output voltage of the inverter (v_{An}) will be $+V_{\mathrm{dc}}$ (positive state) as shown in Fig. 6(a) and (g). During this time interval, diode D_1 is reverse biased and D_2 is ON, so the capacitor C_1 is charged through diode D_2 and the voltage across the capacitor C_2 maintains to be constant. In this state, when the switches S_2 and S_3 are ON, v_{An} will be 0 (zero state) as shown in Fig. 6(b) and (h). In the zero state at positive cycle, the capacitors C_1 and C_2 are connected in parallel through D_1. The capacitor C_2 is charged by the capacitor C_1 with negative polarities by the charge pump circuit to provide the negative voltage level.

In the regions II and III, the negative and zero voltage levels are produced. Fig. 6(c) and (e) shows the equivalent circuit that S_4 and S_1 are ON. The negative voltage is generated, when switch S_4 is turned ON and the voltage across the capacitor C_2 appears at the inverter output voltage ($v_{\mathrm{An}} = -V_{\mathrm{dc}}$) (negative state). The negative output voltage of the inverter is produced by the capacitor C_2. In this state, S_1 is switching simultaneously with S_4. In addition to this, C_1 is charged by the capacitor C_B through S_1 in order to maintain a constant voltage for the capacitor C_1. The voltage across the capacitor C_1 can be kept constant in this state by the modulation strategy. In this period, the circuit operation of the zero state is similar to the zero state of positive half-period of the grid as shown in Fig. 6(b) and (h).

Based on the analysis given above, three sequences exist for the output voltage and current of the proposed inverter.

1) If the sequence is I $\rightarrow$ III, then the inverter is in the unity power factor condition (PF = 1).
2) If the sequence is IV $\rightarrow$ I $\rightarrow$ II $\rightarrow$ III, then the inverter is in the current lagging condition.
3) If the sequence is I $\rightarrow$ IV $\rightarrow$ III $\rightarrow$ II, then the inverter is in the current leading condition.

The aluminum electrolytic capacitors are used for the capacitors C_1 and C_2 of the proposed inverter in the experimental setup. These capacitors have a limited life span because the electrolyte finally dissipates in to the element. Inrush current and voltage stress on the capacitors decrease the lifetime of them. Consequently, in order to reduce the equivalent series resistance (ESR) losses and to ensure the capacitor's lifetime, the capacitance of the aluminum electrolytic capacitors is chosen a little higher than the design values. One of the important elements in the capacitor design is the inrush current of the capacitors. In this case, the charging time constant of capacitor C_2 (τ_{C2}) can be expressed as follows:

$$\tau_{C2} = R_{e1} C_{e1} \tag{5}$$

where R_{e1} and C_{e1} will be as follows:

$$R_{e1} = R_{D1} + R_{S3} + R_{C1} + R_{C2}\,,\; C_{e1} = \frac{C_1 C_2}{C_1 + C_2} \tag{6}$$

in which R_{C1}, R_{C2} are the ESR of the capacitors, R_{S3} denotes the resistor of switch S_3 in the conducting state, and R_{D1} represents the resistor of diode D_1.

The current through capacitors ($i_{\mathrm{Capacitors}}$) is calculated by

$$i_{\mathrm{Capacitors}} = C_{e1} \frac{V_{C1} - V_{C2}}{\tau_{C2}}. \tag{7}$$

According to (5), the charging time constant of C_2 is larger than its natural discharging time constant and $V_{C1} - V_{C2}$ has a very small value in steady state. Due to these analyses and according to (7), the capacitor current value is small in this period and leads to an improvement in the lifespan.

III. Analysis of the Proposed Topology

A. Current Stress Analysis and Capacitors Design

A current stress analysis of the proposed topology is presented in this section. The maximum value of the current stress occurs

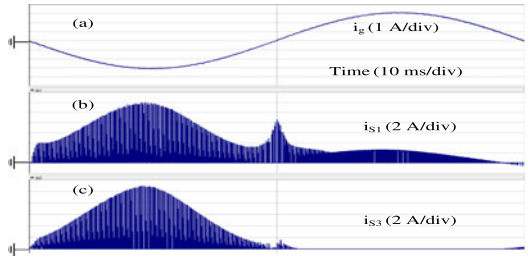

Fig. 7. Simulations of the current of switches: (a) grid current (i_g) [1 A/div], (b) (i_{S1}) [2 A/div], and (c) (i_{S3}) [2 A/div].

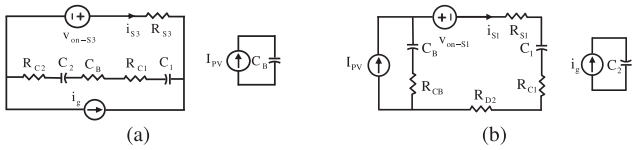

Fig. 8. Equivalent circuit of the proposed converter during (a) zero state and (b) negative state.

on the switches S_1 and S_3, because the capacitor C_1 is charged through switch S_1 and the capacitor C_2 is charged through switch S_3. Using the PSCAD software, simulation results of the current in the switches S_1 and S_3 for an output power of 500 W are shown in Fig. 7. The selected parameters of the simulations are the same as the experimental 500 W prototype. These parameters are listed in Table IV. The maximum value of the current in these switches occurs at the negative state in simulation results as shown in Fig. 7. In the negative half-period of the grid, the circuit shifts between the negative and zero states. During the negative state, the capacitor C_1 is charged by the capacitor C_B, while the capacitor C_2 is discharged by the grid. As a result, the voltage values of the $v_{C2} - v_{C1}$ and $v_{\mathrm{CB}} - v_{C1}$ are increased. When the circuit shifts to zero state, the capacitor C_B is charged by the PV panel, whereas the capacitor C_1 is discharged by the capacitor C_2 in the paralleling mode. Therefore, the voltage difference between the capacitors C_1 and C_B as well as the capacitors C_1 and C_2 is decreased.

The equivalent circuits of the zero and negative states of the proposed topology for the current stress analysis are shown in Fig. 8(a) and (b), respectively.

The power switches are modeled with a resistor (R_s) and a constant voltage source (v_{on}). The capacitor is considered as an ideal capacitor with a series resistor (R_C), the PV panel is regarded as a current source (I_{PV}), and the diode of the topology is modeled with a resistor (R_d). The forward voltage drop of the diodes is neglected. According to the electric circuit theory, the grid voltage in series with a grid-side inductor (L_g) can be equivalent with the current source (i_g) as shown in Fig. 8.

The value of the capacitors C_1 and C_2 determines the maximum current of the power switches. The additional current on the switches S_1 and S_3 is created by the voltage difference between the capacitors C_1, C_2, and C_B. So, by defining two variables $v_{\mathrm{diff},1} = v_{C1} - v_{C2} - v_{\mathrm{on}}$ and $v_{\mathrm{diff},2} = v_{\mathrm{CB}} - v_{C1} - v_{\mathrm{on}}$, the state equation for zero and negative states can be taken separately.

According to Fig. 8(a), at the zero state

$$\frac{dv_{\mathrm{diff},1}}{\mathrm{d}t} = \frac{v_{\mathrm{diff},1} - R_{s3} i_g}{(R_{e1} + R_{s3})C_{e1}} \tag{8}$$

$$\frac{dv_{\mathrm{diff},2}}{\mathrm{d}t} = \frac{I_{\mathrm{PV}}}{C_B} - \frac{v_{\mathrm{diff},1} - R_{s3} i_g}{(R_{e1} + R_{s3})C_1}. \tag{9}$$

According to Fig. 8(b), in the negative state

$$\frac{dv_{\mathrm{diff},1}}{\mathrm{d}t} = \frac{R_{\mathrm{Cb}} I_{\mathrm{PV}} + v_{\mathrm{diff},2}}{(R_{\mathrm{cb}} + R_{e2})C_1} + \frac{i_g}{C_2} \tag{10}$$

$$\frac{dv_{\mathrm{diff},2}}{\mathrm{d}t} = \frac{I_{\mathrm{PV}}}{C_B} + \frac{R_{\mathrm{cb}} I_{\mathrm{PV}} - v_{\mathrm{diff},2}}{R_{e2} C_{e2}} \tag{11}$$

where in (8)–(11), R_{e2} and C_{e2} will be as follows:

$$R_{e2} = R_{D2} + R_{S1} + R_{C1} + R_{\mathrm{CB}},\ C_{e2} = \frac{C_1 C_B}{C_1 + C_B}. \tag{12}$$

By using the averaging method at the switching cycle T_s, and linearizing (8)–(11), the average value of i_{S1} and i_{S3} at the negative and zero states is equal to (13) and (14), respectively:

$$\begin{aligned}\frac{dv_{\mathrm{diff},1}}{\mathrm{d}t} &= (1 + s(t))\frac{v_{\mathrm{diff},1} - R_{s3} i_g}{(R_{e1} + R_{s3})C_{e1}} \\ &\quad - s(t)\left(\frac{R_{\mathrm{CB}} I_{\mathrm{PV}} + v_{\mathrm{diff},2}}{(R_{\mathrm{cB}} + R_{e2})C_1} + \frac{i_g}{C_2}\right)\end{aligned} \tag{13}$$

$$\begin{aligned}\frac{dv_{\mathrm{diff},2}}{\mathrm{d}t} &= (1 + s(t))\left(\frac{I_{\mathrm{PV}}}{C_B} - \frac{v_{\mathrm{diff},1} - R_{s3} i_g}{(R_{e1} + R_{s3})C_1}\right) \\ &\quad - s(t)\left(\frac{I_{\mathrm{PV}}}{C_B} + \frac{R_{\mathrm{cB}} I_{\mathrm{PV}} - v_{\mathrm{diff},2}}{R_{e2} C_{e2}}\right)\end{aligned} \tag{14}$$

where $s(t)$ denotes the switching state function given as follows:

$$s(t) = \begin{cases} 1, & \text{when the circuit is at positive state} \\ 0, & \text{when the circuit is at zerostate} \\ -1, & \text{when the circuit is at negative state.} \end{cases} \tag{15}$$

Rearranging (13) and (14) and using the averaging method in the switching cycle T_s, we have

$$\begin{aligned}&\frac{\mathrm{d}}{\mathrm{d}t}\langle v_{\mathrm{diff},1}\rangle_{T_s} - \frac{\langle v_{\mathrm{diff},1}\rangle_{T_s}(1 + \mathrm{d}(t))}{(R_{e1} + R_{s3})C_{e1}} + \frac{\langle v_{\mathrm{diff},2}\rangle_{T_s}\mathrm{d}(t)}{(R_{e2} + R_{\mathrm{cB}})C_1} \\ &= -\frac{R_{s3}\langle i_g\rangle_{T_s}(1 + d(t))}{(R_{e1} + R_{s3})C_{e1}} - \frac{(R_{\mathrm{cB}} I_{\mathrm{PV}})\mathrm{d}(t)}{(R_{e2} + R_{\mathrm{cB}})C_1} - \frac{\langle i_g\rangle_{T_s}\mathrm{d}(t)}{C_2}\end{aligned} \tag{16}$$

$$\begin{aligned}&\frac{\mathrm{d}}{\mathrm{d}t}\langle v_{\mathrm{diff},2}\rangle_{T_s} + \frac{\langle v_{\mathrm{diff},2}\rangle_{T_s}\mathrm{d}(t)}{R_{e2} C_{e2}} + \frac{\langle v_{\mathrm{diff},1}\rangle_{T_s}(1 + \mathrm{d}(t))}{(R_{e1} + R_{s3})C_1} \\ &= \frac{I_{\mathrm{PV}}}{C_B} - \frac{R_{s3}\langle i_g\rangle_{T_s}(1 + \mathrm{d}(t))}{(R_{e1} + R_{s3})C_1} - \frac{(R_{\mathrm{cB}} I_{\mathrm{PV}})d(t)}{R_{e2} C_{e2}}\end{aligned} \tag{17}$$

where $d(t)$ and $i_g(t)$ are

$$\mathrm{d}(t) = M \sin \omega t \tag{18}$$

$$\mathrm{i}_g(t) = I_m \sin \omega t \tag{19}$$

where ω denotes the angular frequency of the output current, M is the ratio of the dc voltage and grid voltage, and I_m represents the peak output current of the inverter.

The average current of i_{S1} and i_{S3} during T_s can be found as follows:

$$\langle i_{s_1}\rangle_{T_2} = \frac{\langle v_{\text{diff},1}\rangle_{T_s} + R_{s3}\langle i_g\rangle_{T_s}}{R_{e1}+R_{s3}} \tag{20}$$

$$\langle i_{s_3}\rangle_{T_2} = \frac{\langle v_{\text{diff},2}\rangle_{T_s} + R_{\text{cB}} I_{\text{PV}}}{R_{e2}}. \tag{21}$$

The simulation results of the current flowing through the switches S_1 and S_3 for the output power 500 W are shown in Fig. 7. The value of the current that passes through S_1 and S_3 to reach to its maximum at the negative state is shown in this figure too. At the negative state, $\langle v_{\text{diff},1}\rangle_{T_s} = 0$, $\langle v_{\text{diff},2}\rangle_{T_s} = 0$, $\langle i_g\rangle_{T_s} = -I_m$ and $d(t) = -M$, the maximum current stress of the switches S_1 and S_3 is

$$\langle i_{s_1,\max}\rangle_T = \frac{1}{2}\left(\frac{C_1}{C_1+C_2}+1\right)\left(\frac{M\,I_m}{1-M}+\frac{T_s}{R_{e1}\,C_{e1}}\frac{1-M}{2}\right) \tag{22}$$

$$\langle i_{s_3,\max}\rangle_T = \frac{1}{2}\left(\frac{C_1}{C_1+C_B}+1\right)\left(\frac{M\,I_m}{1-M}+\frac{T_s}{R_{e_2}\,C_{e_2}}\frac{1-M}{2}\right). \tag{23}$$

Equations (22) and (23) indicate that the values of $C_1/(C_1+C_2)$ and $C_1/(C_1+C_B)$ should be calculated small enough, and the values of the $R_{e1}C_{e1}$ and $R_{e2}C_{e2}$ should be smaller than the switching period in order to minimize the current stress on the switches. Therefore, there is a tradeoff between the current stress on the switches and the size of the switched capacitors. To achieve these objectives, the capacitors C_1, C_2, and C_B must be set to $C_1 < C_2$ and $C_1 < C_B$ to reduce $C_1/(C_1+C_2)$ and $C_1/(C_1+C_{\text{B}})$, respectively. The value of $C_1/(C_1+C_2)$ and $C_1/(C_1+C_B)$ is almost set to 1/4 by considering the capacitance of the capacitors, and hence, $i_{S1,\max} = 4I_m$ and $i_{S3,\max} = 4I_m$. These values can be limited by a small resistor or a small inductor between the capacitors if needed.

According to this analysis, the current flowing through the capacitors of C_1 and C_B has the same value of the current flowing through switch S_3 and S_1, respectively. The relationship between the voltage and current passing through the capacitors is calculated by

$$i_C = C\frac{\Delta v_C}{\Delta t}. \tag{24}$$

The required capacitance of C_1 and C_B for the proposed inverter can be derived by equaling the capacitor power magnitude to the grid power ripple magnitude. The capacitance C_1 and C_B can be calculated as follows:

$$C_{1\text{ or }B} = \frac{I_{C_{1\text{ or }B}\ (\max)}}{(\hat{V}_r\ V_n)\,f} \tag{25}$$

where $I_{C1\max}$ and $I_{CB\max}$ are the maximum current that passes through the capacitors C_1 and C_B, respectively. $\hat{V}_r$, V_n, and f are the capacitor voltage ripple magnitude, nominal voltage on the capacitor, and the frequency during maximum current, respectively. By applying suitable values for these parameters in (25), the capacitance of C_1 and C_B is calculated.

TABLE I
DUTY RATIO OF EACH CONDUCTING DEVICE

Semiconductor devices	Duty ratio (d)	
	Positive cycle ($v_g > 0$)	Negative cycle ($v_g < 0$)
S_1	$M \sin\omega t$	$M \sin\omega t$
S_2	1	$1–M \sin\omega t$
S_3	$M \sin\omega t$	$1–M \sin\omega t$
S_4	0	$M \sin\omega t$
D_1	0	$M \sin\omega t$
D_2	$M \sin\omega t$	0

B. Conduction and Switching Losses of Power Devices

During the positive power cycle, the grid current flows through switches S_1 and S_2 and the capacitor C_1 is charged through diode D_2 at the positive state as shown in Fig. 6(a) and (g). At zero state, the grid current flows through S_2 and S_3 and the capacitor C_2 is charged through diode D_1. In this cycle, there are two switches on the grid current path and one diode is conducting in each state. In the negative cycle of the grid, the grid current flows through S_4. The capacitor C_1 is charged through diode D_2 and switch S_1 at the negative state as shown in Fig. 6(c) and (e).

The voltage drop of the power devices can be derived by

$$\text{MOSFET}: v_{\text{DS}}(t) = i(t)R_{\text{DS}} \tag{26}$$

$$\text{Diode}: v_{\text{AK}}(t) = V_F + i(t)R_{\text{AK}} \tag{27}$$

where v_{DS} is the drain source voltage drop of the MOSFET, R_{DS} is the drain source resistance of the MOSFET during on the state operation, v_{AK} is the anode cathode voltage drop of the diode, V_F is the equivalent voltage drop under zero current condition of the diode, R_{AK} is the anode cathode resistance of the diode during the on state, and $i(t)$ is the grid current.

The duty ratio of the conducting devices is given in Table I using the unipolar SPWM strategy in the proposed grid-connected inverter. The average value of the conduction losses of the MOSFET switch ($P_{\text{MOSFET_Cond}}$) during half of the fundamental period is calculated by

$$P_{\text{MOSFET_Cond}} = \frac{1}{\pi}\int_0^{\pi} v_{\text{DS}}(t)\,i(t)\,d_{\text{MOSFET}}(t)\,d\omega t. \tag{28}$$

The average value of the conduction loss in the diode ($P_{\text{Diode_Cond}}$) during the on state mode is calculated by

$$P_{\text{Diode_Cond}} = \frac{1}{\pi}\int_0^{\pi} v_{\text{AK}}\,i(t)d_{\text{Diodes}}(t)d\omega t = \frac{1}{\pi}\int_0^{\pi}(V_F + i(t)R_{\text{AK}})i(t)d_{\text{Diodes}}(t)d\omega t. \tag{29}$$

The total conduction losses of the MOSFET switches and diodes ($P_{\text{Proposed_Cond}}$) for the proposed inverter during a

TABLE II
SPECIFICATIONS AND POWER DEVICES FOR EFFICIENCY EVALUATION

Parameters	Value
Input voltage	400 V
Grid voltage/frequency	220 V/50 Hz
Rated power	500 W
AC output current (RMS)	2.3 A
Switching frequency	24 kHz
Duty ratio (M)	0.78
MOSFET switches	C2M0080120D, $R_{\mathrm{DS}} = 0.05\,\Omega$
Diode (D_1–D_2)	C3D10060A, $V_F = 0.7$ V, $R_{\mathrm{AK}} = 0.01\,\Omega$

fundamental period can be calculated from

$$\begin{aligned} P_{\mathrm{Proposed_Cond}} &= P_{\mathrm{MOSFETs}} + P_{\mathrm{Diodes}} \\ &= 4\left(\frac{4MR_{\mathrm{DS}}I^2{}_m}{3\pi}\right) + \left(\frac{R_{\mathrm{DS}}I^2{}_m}{2}\right) \\ &\quad + \left(R_{\mathrm{DS}}I^2{}_m - \frac{4MR_{DS}I^2{}_m}{3\pi}\right) \\ &\quad + 2\left(\frac{MV_FI_m}{2} + \frac{4MR_{\mathrm{AK}}I^2{}_m}{3\pi}\right) = 3.1\,\mathrm{W}. \end{aligned} \tag{30}$$

The device manufacturer and circuit parameters for efficiency evaluation of proposed inverter are listed in Table II.

In silicon carbide power MOSFET switches, the recovery current of the diodes is eliminated and therefore the switching losses for the diodes are negligible. The switching losses of the MOSFET switch can be found as follows:

$$P_{\mathrm{MOSFET_sw}} = f_{\mathrm{sw}}E_{\mathrm{oss}}V_F \tag{31}$$

where E_{oss} is the stored energy that can be achieved from the datasheet that is equal to 45 μJ. The total switching losses of the switches in the proposed inverter can be derived as follows:

$$P_{\mathrm{Total-sw}} = 4f_{\mathrm{sw}}E_{\mathrm{oss}}V_F = 3.46\,\mathrm{W}. \tag{32}$$

C. Conduction Losses in the Capacitors

The ESR of the capacitors of the proposed inverter is achieved from aluminum electrolyte capacitor datasheets and it is divided into two parts. The first part of the conduction losses in the capacitors is similar to the conventional transformerless inverters including FB, H5, HERIC, etc. The second part of the conduction losses is related to the inrush current during the charging of the capacitors. These losses can be defined as follows:

$$P_{\mathrm{CAP_Cond_1}} = \frac{2(R_{C1} + R_{\mathrm{CB}})}{\pi}\int_0^{\pi} d_c(t)\, i^2{}_{S1}(t)\; d\omega t \tag{33}$$

$$P_{\mathrm{CAP_Cond_2}} = \frac{2(R_{C1} + R_{C2})}{\pi}\int_0^{\pi} d_c(t)\, i^2{}_{S3}(t)\; d\omega t \tag{34}$$

where $d_c(t)$ is the duty ratio of the capacitor. The aluminum electrolytic capacitors are used in the experimental hardware. The simulation result of this loss with PSCAD software is totally around 3.1 W at 500 W prototype.

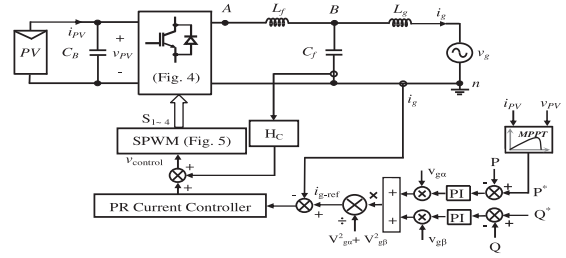

Fig. 9. Control block diagram of the proposed single-phase grid-tied inverter based on single-phase PQ theory.

D. Control Scheme

The control strategy of the proposed grid-tied single-phase inverter is shown in Fig. 9. It contains two cascaded loops [21]: the first loop is an inner control loop, which has the responsibilities to generate a sinusoidal current and the outer control loop is implemented for the current reference generation, where the power is controlled. A proportional resonant (PR) controller provide an infinite gain at the resonant frequency (f_{res}) and can eliminate the steady state error when tracking a sinusoidal signal, which is an index of power quality. Due to these features, the PR controller is selected instead of the PI controller in the current control loop in this topology [22]. The transfer function of this controller can be found as follows:

$$G_{\mathrm{PR}}(s) = K_p + \frac{2K_r}{s^2 + \omega^2} \tag{35}$$

where k_p is the proportional gain, k_r is the fundamental resonant gain, and ω is the resonant frequency.

The power control loop requires orthogonal signal generation systems to create quadrature components ($v_{g\alpha}$, $v_{g\beta}$ and $i_{g\alpha}$, $i_{g\beta}$) corresponding to the grid voltage v_g and grid current i_g, and then it generates a current reference, which is used in the inner current control loop. According to the single-phase *PQ* theory [23], [24], the current reference can be produced by regulating the active and reactive powers. The active power (P) and reactive power (Q) for the proposed topology can be calculated by [24]

$$\begin{aligned} P &= \frac{v_{g\alpha}i_{g\alpha} + v_{g\beta}i_{g\beta}}{2} \\ Q &= \frac{v_{g\alpha}i_{g\alpha} - v_{g\beta}i_{g\beta}}{2} \end{aligned} \tag{36}$$

where $v_{g\alpha}$, $v_{g\beta}$, $i_{g\alpha}$, and $i_{g\beta}$ are the α and β components of grid voltage and current, respectively. The active power and reactive power references (P^* and Q^*) can be tuned by the operators {*R*–3} or in the control unit, when the MPPT control is activated. The current reference can be computed in the $\alpha\beta$-reference frame, which simplifies the overall control. If PI controllers are used for power regulations, the grid current reference ($i_{g\text{-ref}}$) can be derived as follows [24]:

$$i_{g-\mathrm{ref}} = \frac{1}{v^2{}_{g\alpha} + v^2{}_{g\beta}}\begin{bmatrix} v_{g\alpha} & v_{g\beta} \end{bmatrix}\begin{bmatrix} G_p(s)\;(P - P^*) \\ G_q(s)\;(Q - Q^*) \end{bmatrix} \tag{37}$$

where $G_{\mathrm{p}}(s)$ and $G_{\mathrm{q}}(s)$ are the PI controllers for active power and reactive power, respectively.

The *LCL* filter is adopted as the grid interfaced filter in this proposed topology. High output current quality in the proposed inverter can be obtained if the output filter is configured correctly. The first design consideration is the calculation of the filter parameters, which can be determined by current ripple and filter values [25]. The inverter-side inductor (L_f) value is calculated by considering 10–20% of the ripple on the output current, which is given by

$$L_f = \frac{(v_{\rm dc} - v_{\rm An})\,(M\,\sin\omega t)}{f_{\rm sw}\;\Delta i_L} \tag{38}$$

where $f_{\rm sw}$ is the switching frequency and $\Delta i_{\rm L}$ represents the peak-to-peak ripple current on the L_f. The inverter output voltage ($v_{\rm An}$) can be calculated as follows:

$$v_{\rm An} = M\,V_{\rm dc}\,\sin\omega t. \tag{39}$$

By replacing (39) with (38) and simplifying it, we have

$$L_f = \frac{(v_{\rm dc})\,(RF)}{f_{\rm sw}\;\Delta i_L} \tag{40}$$

where RF is the ripple current and can be calculated from

$$RF = M\,\sin\omega t - M^2\,\sin^2\omega t. \tag{41}$$

The maximum achievable value of modulation index (*M*) is $RF_{\rm max} = 0.25$ [26]. The maximum value of the filter capacitor is calculated by (42), limiting to be less than 5% of the nominal value [27]

$$C_{f,\max} = \frac{0.05P_n}{2\pi f V^2{}_{\rm rms}} \tag{42}$$

where P_n is the nominal power, $V_{\rm rms}$ denotes the root mean square (RMS) grid voltage, and *f* presents the grid frequency. There is a relation between the inverter-side inductor (L_f) and the grid side (L_g). This value is determined with the ratio between the ripple attenuation (*r*) as described in [28]

$$L_g = rL_f. \tag{43}$$

The grid-side inductor ($L_{\rm g}$) value can be determined by

$$10f \le f_{\rm res} \le 0.5f_{\rm sw}. \tag{44}$$

The resonant frequency for the *LCL* filter is given by

$$f_{\rm res} = (1/2\pi)\sqrt{(L_f + L_g)/L_f L_g C_f}. \tag{45}$$

The second consideration is the current control strategy effect on the output filter design. In the closed-loop control system, the combination of *L* and *C* can cause a resonance problem, which may lead to instability of the controller. The active damping is used to smooth the resonance peak of the *LCL* filter as shown in Fig. 9 [29], [30]. A block diagram of the control system is shown in Fig. 10. The Bode diagram of the transfer function from $v_{\rm cref}$ to i_g is defined by *G*(*s*). This diagram is shown in Fig. 11 in order to demonstrate the effect of active damping by the filter capacitor current ($H_c i_c$)

$$G(s) = \frac{K_{\rm PWM}\;G_1(s)}{1 + H_C K_{\rm PWM} C_f L_g G_1(s)\,s^2} \tag{46}$$

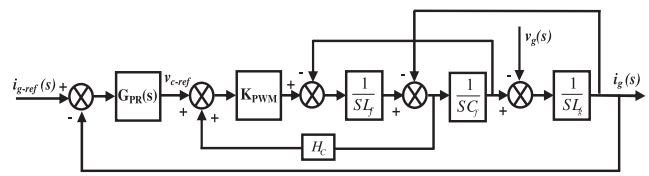

Fig. 10. Control diagram of the injected current with capacitor current feedback active damping.

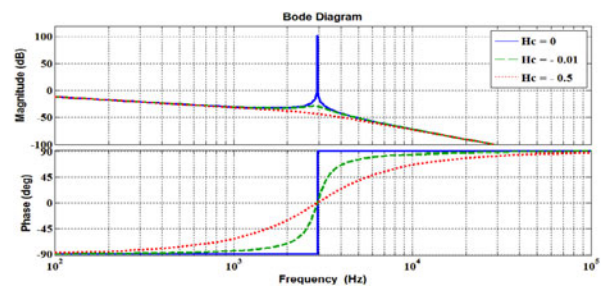

Fig. 11. Bode plot of the system in the case of different values for the active damping gain H_C.

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGY WITH THE CONVENTIONAL TRANSFORMERLESS TOPOLOGIES

Converter	Semiconductor devices				Switches in the current path	THDi (%)
	Switches	Diodes	*C*	*L*		
H5	5	0	1	3	3	2
HERIC	6	0	1	3	2	1.9
CM in [31]	7	2	2	2	4	2.5
CM in [32]	6	0	3	2	3	2.8
CM in [33]	6	6	2	2	3	2.2
Proposed	4	2	3	2	2	2.1

where

$$G_1(s) = \frac{1}{sL_g + sL_f(1 + s^2 L_g C_f)} \tag{47}$$

and $K_{\rm pwm} = 1$ and H_C is the active damping gain. The effect of H_C is shown in Fig. 11, where a high value of H_C shows better resonance peak damping capabilities.

E. Comparison With Other Known Topologies

A comparison of the transformerless inverter structures with respect to number of semiconductor devices, passive elements, THD of the current, and number of switches in the current path is listed in Table III. This comparison includes conventional H5, HERIC inverter, and several common ground transformerless inverters like [31]–[33] with the proposed inverter. It can be seen from Table III that the proposed topology utilizes the least amount of active and passive components compared to the other topologies, which reduces the number of driver circuits, complexity of control, and power losses of the inverter. In

TABLE IV
EXPERIMENTAL PARAMETERS FOR THE 500 W PROTOTYPE

Parameter	Value	Parameter	Value
Power rating (P)	500 W	Capacitance (C_1)	220 μF, 500 V
Input voltage (V_{dc})	400V	Capacitance (C_2)	330 μF, 500 V
Output voltage (v_{Bn})	220 V (RMS)	L filter (L_f)	4 mH
Input capacitor (C_B)	470 μF, 500 V	C filter (C_f)	2.2 μF
Power switches ($S_1 - S_4$)	C2M0080120D, SiC MOSFET	L_g	2 mH
Diodes (D_1, D_2)	C3D10060A Schottky Diode	Switching frequency (f_s)	24 kHz

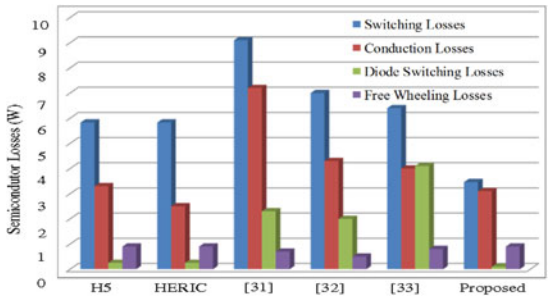

Fig. 12. Total semiconductor power losses distribution for the H5, HERIC, [31]–[33] and the proposed topologies at rated power.

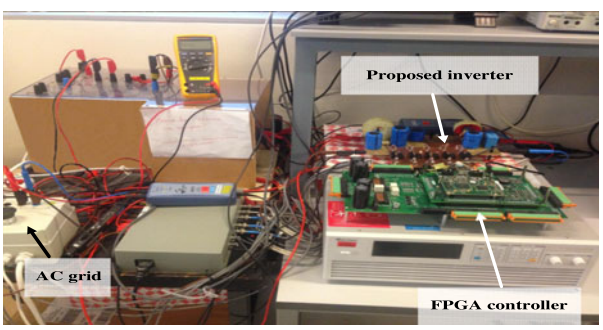

Fig. 13. Laboratory prototype of the single-phase grid-tied proposed inverter used in the experiment.

this comparison, it is shown that the H5 and HERIC inverters are using extra switches to disconnect the grid side from the dc side, and this disconnection is incomplete due to the parasitic capacitance of switches. Therefore, the high-frequency CM current flows through parasitic capacitors. Thus, these topologies need extra filters to absorb the CM current according to Table III and the analysis given in Section I. Due to the configuration of the charge pump circuit in the proposed topology, the CM current is completely eliminated without extra filters. In addition, the dc voltage used in the proposed inverter is the same as the conventional FB inverter, and only half of the dc voltage used in conventional HB, NPC, and ANPC inverters, while the performance in eliminating the CM current is better than the FB-based inverters. The THD of the grid currents for these topologies is listed in Table III. It can be seen that all the single-phase transformerless topologies have similar THD of the grid current.

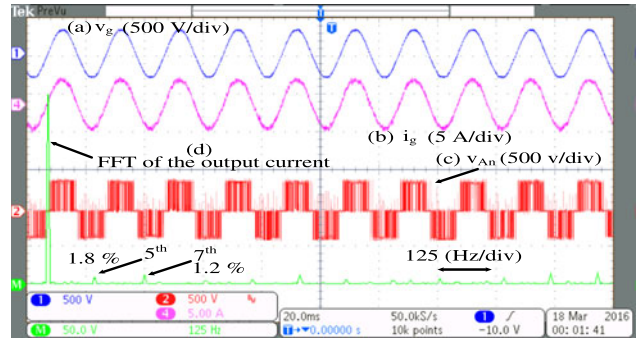

Fig. 14. Experimental results of the proposed topology with unity power factor (PF = 1) operation. (a) v_g [500 V/div], (b) i_g [5 A/div], (c) v_{An} [500 V/div], and (d) fast Fourier transform analysis of i_g [50 V/div and 125 Hz/div].

The number of switches in the current path is related to the conduction losses. It can be seen from Table III that the number of switches in the current path and semiconductor devices of the CM inverter [31] are larger than the other topologies. Fig. 12 shows the power semiconductor losses distribution according to the switching frequency at the rated power of all inverter topologies listed Table III with the same circuit parameters. The switching losses are calculated based on the datasheet of the devices. The calculation process is studied in detail in the literature [34]. The total semiconductor losses consist of the switching losses, conduction losses, switching losses of diode, and freewheeling losses. It is important to know that the conduction loss internal SiC diode of MOSFET implemented in the proposed inverter is less than the conduction loss of the IGBT body diode used in the H5, [31]–[33]. As shown in Fig. 12, the H5 and HERIC topologies have almost the same switching losses, because the number of high frequency switches is the same. The proposed topology has the lowest switching losses according to the analysis presented in Section III. According to Table III, the conduction losses of [31] are high because many switches are used in the current path during the inverter operation. Freewheeling losses of all inverter topologies are almost the same. As a result, Shen *et al.* [31] have the highest total losses and the proposed topology has the lowest losses because of low switching and conduction losses at 500 W output power, which validate the theoretical analysis.

IV. EXPERIMENTAL VERIFICATION AND DISCUSSION

In order to verify the feasibility of the proposed topology, a 500 W, single-phase transformerless grid-tied inverter has been built in the laboratory and experimentally tested. A photograph of the proposed transformerless inverter prototype is depicted in Fig. 13. The configuration and parameters used for the experimental tests are listed in Table IV. The experimental results of the proposed grid-connected inverter with unity power factor (PF = 1) operation are presented in Fig. 14. The grid voltage has the same phase as the injected grid current as shown in Fig. 14(a) and (b). Fig. 14(c) shows that the inverter output voltage v_{An} has three levels as $+V_{dc}$, 0, and $-V_{dc}$ without the *LCL*-filter circuit. This determines that the proposed topology is

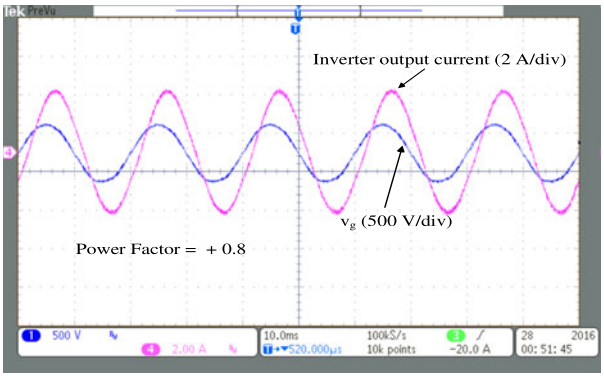

Fig. 15. Experimental results of the proposed topology with lagging power factor operation. (a) v_g [500 V/div] and (b) i_g [2 A/div].

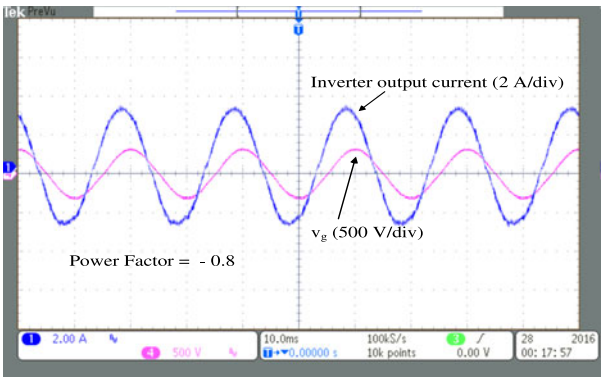

Fig. 16. Experimental results of the proposed topology with leading power factor operation. (a) v_g [500 V/div] and (b) i_g [2 A/div].

modulated with unipolar SPWM. From Fig. 14, it is clear that the output current and voltage of the proposed inverter are highly sinusoidal with low harmonic distortion due to the three-level inherency of the output voltage. The current harmonic distribution is demonstrated in Fig. 14(d). It can be seen that the 5th-, 7th-, and 11th-order harmonics are very low and the output voltage and current of the topology are very close to be sinusoidal. The experimental results for the THD measurement of the grid current are equal to 2.1% in unity power factor operation and it is lower than the recommended value by the IEEE STD 519-1992 [35]. The RMS value of the current injected to the grid is equal to 2.3 A, and the output power is 500 W.

Figs. 15 and 16 demonstrate the experimental results for the inverter operating under current lagging condition (PF = + 0.8) and leading condition (PF = –0.8), respectively. The partial enlargement of the grid current i_g, grid voltage v_g, and three level output voltage v_{An} is provided in Fig. 17. It is clear that the pulse duration of the output voltage (v_{An}) is in agreement with the switching frequency.

The experimental results of the voltage across the switches S_1, S_2, S_3, and S_4 under 400 V input voltage conditions are shown in Fig. 18. The voltage stress of the switches S_1, S_2, and S_3 is the same as the input dc voltage and on the switch S_4 is double of the input voltage. The voltage stress of the capacitors and diodes is shown in Fig. 19. From the experimental waveforms

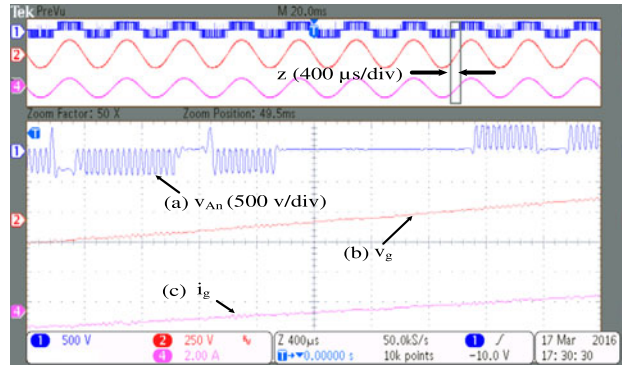

Fig. 17. Experimental enlarged results of the proposed topology. (a) v_{An} [500 V/div], (b) v_g [250 V/div], and (c) i_g [5 A/div], time [400 μs/div].

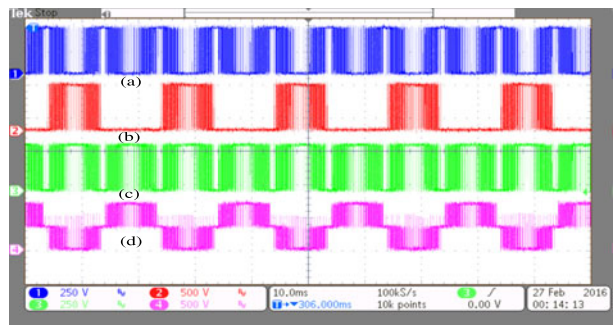

Fig. 18. Experimental results for drain source voltage of switches. (a) v_{S1} [250 V/div], (b) v_{S2} [500 V/div], (c) v_{S3} [250 V/div], and (d) v_{S4} [500 V/div].

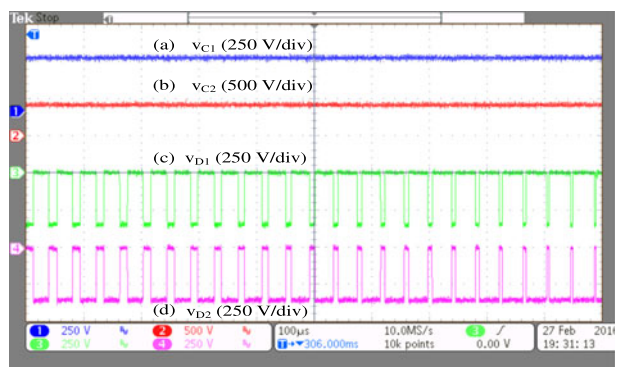

Fig. 19. Experimental results of the capacitor and diode voltages. (a) v_{C1} [250 V/div], (b) v_{C2} [500 V/div], (c) v_{D1} [250 V/div], and (d) v_{D2} [250 V/div].

of the output voltage, it can be seen that there are no voltage overshoots across the MOSFET switches.

Fig. 20(a)–(c) shows the experimental waveforms of the grid voltage v_g, the grid current i_g, and the CM voltage v_{CM} in the proposed topology. It can be seen that by applying unipolar modulation SPWM strategy, the CMV of the proposed inverter has been kept constant. As a result, the CM current of the proposed inverter is eliminated due to the configuration of the charge pump circuit. Therefore, this solution with a charge pump circuit provides a new idea for using the proposed inverter for PV applications.

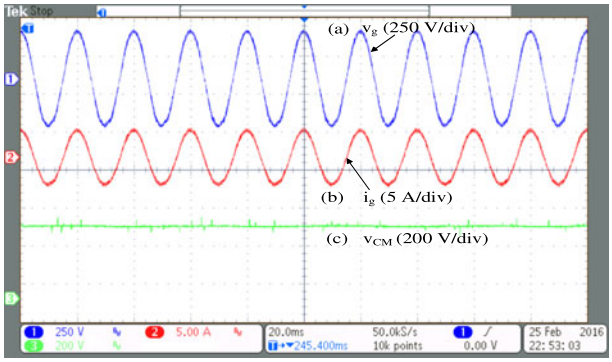

Fig. 20. Experimental results of the proposed topology. (a) v_g [250 V/div], (b) i_g [5 A/div], and (c) CMV [200 V/div].

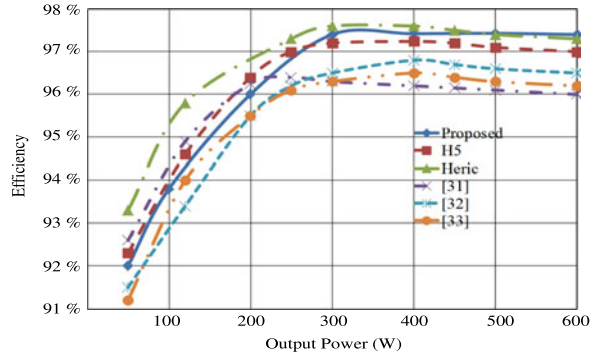

Fig. 22. Efficiency comparison for transformerless topologies under different output power and unit power factor.

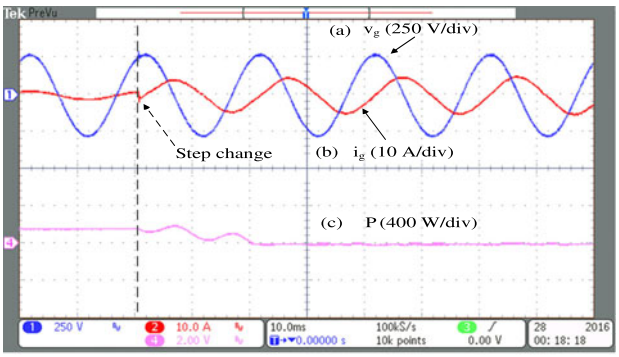

Fig. 21. Experimental results of the proposed topology in dynamic state. (a) v_g [250 V/div], (b) i_g [10 A/div], and (c) active power (*P*) [400 W/div].

The performance of the control strategy is confirmed by applying a step change to the proposed inverter. A PR current controller is adopted with $k_i = 2000$ and $k_p = 20$ as shown in (35). Fig. 21 shows the performance of the proposed inverter under the load step change. It has been demonstrated that the proposed inverter can track step change when the output power is decreased from 200 W to zero. As it can be seen, this test demonstrates the effectiveness of the power control strategy used in this paper in terms of fast response.

As described in the previous section, the efficiency of the proposed inverter mainly relies on the losses of the power devices. Fig. 22 shows the efficiency of the H5, HERIC, [31]–[33] and the proposed inverter $\{R\text{–}2\}$ having the same output power and unity PF. The efficiency comparison curves illustrate the experimental results under the same dc-link voltages, output power, switching frequency, and 220 $V_{\rm rms}$ ac output voltage conditions. The only difference is the components. IGBTs are used in the H5, HERIC, [31]–[33], while SiC MOSFETs are used in the proposed inverter. A VOLTECH PM300 power analyzer has been used to measure the efficiency of the proposed inverter. It may be noted that the efficiency diagram covers the total power device losses and the filter inductor losses. The curves show that the HERIC has the highest efficiency for the low power applications but the leakage current characteristic is worse in comparison to the proposed topology. The efficiency of the proposed inverter is lower than the H5 and a little less than the HERIC topology at low power, while it is better at high power. The measured maximum efficiency of the proposed inverter is around 97.4% at 500 W. The experimental efficiency of the proposed inverter confirms the power loss calculation in Section III-B . As shown in (48), the California Energy Commission (CEC) efficiency is calculated combining different weighted factors at different output power levels [36]

$$\eta_{\rm CEC} = 0.04\,\eta_{10\%} + 0.05\,\eta_{20\%} + 0.12\,\eta_{30\%} + 0.21\,\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}. \quad (48)$$

The calculated CEC efficiency of the proposed transformerless inverter is 97.2%. As a result, the conduction loss in the semiconductors of the proposed inverter is similar to the H5 and HERIC inverters and the total device loss for the HERIC topology at low power is higher than the proposed inverter. Hence, the proposed inverter reduces the output current ripple in addition to maintain a high efficiency without leakage current.

V. Conclusion

This paper proposed a new single-phase transformerless inverter for a grid-tied PV system using a charge pump circuit concept. The concept is proposed to generate the negative output voltage in the proposed inverter. This new topology generates a three level output voltage by employing unipolar SPWM. The negative terminal of the proposed topology is the same as the neutral line in the grid; thus, the leakage current is well suppressed and the transformer is eliminated. The proposed topology has also the ability to deliver reactive power into the grid. In addition, the proposed topology can be realized with a minimum number of components; hence, a higher power density can be achieved with lower design cost. Compared to other existing transformerless topologies, the performance depicted by the proposed inverter is good. A theoretical analysis performed and it is validated by experimental results for a grid-connected inverter prototype. The proposed topology is verified with a 500 W prototype. The maximum efficiency of the proposed inverter is measured to be 97.4%. Experimental results and loss calculations demonstrate the validity of the proposed inverter with lower

THD for the grid-connected inverter. It can be concluded that the proposed topology is suitable for a grid-tied transformerless inverter.

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Jaber Fallah Ardashir was born in Tabriz, Iran, in 1987. He received the B.Sc. degree in power electrical engineering from Azerbaijan Shahid Madani University, Tabriz, Iran, in 2010, and the M.Sc. degree in power electrical engineering from Zanjan University, Zanjan, Iran, in 2012. He received the Ph.D. degree from the University of Tabriz, Tabriz, Iran, in 2017.

In 2016, he joined the Faculty of Electrical Engineering, Islamic Azad University of Tabriz. His current research interests include power electronic converters and renewable energy systems.

Mehran Sabahi was born in Tabriz, Iran, in 1968. He received the B.Sc. degree in electronic engineering from the University of Tabriz, Tabriz, in 1991, the M.Sc. degree in electrical engineering from Tehran University, Tehran, Iran, in 1994, and the Ph.D. degree in electrical engineering from the University of Tabriz in 2009.

In 2009, he joined the Faculty of Electrical and Computer Engineering, University of Tabriz, where he has been an Associate Professor since 2015. His current research interests include power electronic converters and renewable energy systems.

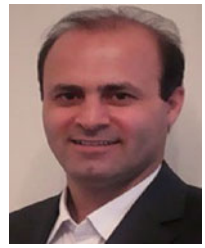
Seyed Hossein Hosseini (M'93) was born in Marand, Iran, in 1953. He received the M.S. degree from the Faculty of Engineering, University of Tabriz, Tabriz, Iran, in 1976, and the D.E.A. and Ph.D. degrees from the Institute National Polytechnique de Lorraine, Nancy, France, in 1978 and 1981, respectively, all in electrical engineering.

In 1982, he joined the University of Tabriz as an Assistant Professor in the Department of Electrical Engineering. From September 1990 to September 1991, he was a Visiting Professor at the University of Queensland, Australia. From 1990 to 1995, he was an Associate Professor at the University of Tabriz. Since 1995, he has been a Professor in the Department of Electrical Engineering, University of Tabriz. From September 1996 to September 1997, he was a Visiting Professor at the University of Western Ontario, London, ON, Canada. His research interests include power electronics, application of power electronics in renewable energy systems and electrified railway systems, and FACTS devices.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998 at Aalborg University. His current research interests include power electronics and applications such as in wind turbines, photovoltaic systems, reliability, harmonics, and adjustable-speed drives.

Prof. Blaabjerg has received 17 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014. He was Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He was nominated in 2014 and 2015 by Thomson Reuters as one of the 250 most cited researchers in engineering in the world.



Ebrahim Babaei (M'10–SM'16) was born in Ahar, Iran, in 1970. He received the B.S. degree in electronic engineering and the M.S. degree in electrical engineering from the Department of Engineering, University of Tabriz, Tabriz, Iran, in 1992 and 2001, respectively, where he also received the Ph.D. degree in electrical engineering from the Department of Electrical and Computer Engineering in 2007.

He was an Assistant Professor from 2007 to 2011, an Associate Professor from 2011 to 2015, and has been a Professor since 2015 at the University of Tabriz. He is the author of more than 320 journal and conference papers. He also holds 16 patents in the area of power electronics. His current research interests include the analysis, modeling, design, and control of power electronic converters and their applications, renewable energy sources, and FACTS devices.

Prof. Babaei has been the Editor-in-Chief of the *Journal of Electrical Engineering* of the University of Tabriz since 2013. He is also currently an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE TRANSACTIONS ON POWER ELECTRONICS. He has received the Best Researcher Award from the University of Tabriz several times. He has been included in the Top One Percent of the World's Scientists and Academics according to Thomson Reuters' list in 2015.

Gevork B. Gharehpetian (SM'96) received the B.S. degree from Tabriz University, Tabriz, Iran, in 1987, the M.S. degree from Amirkabir University of Technology (AUT), Tehran, Iran, in 1989, and the Ph.D. degree from Tehran University, Tehran, in 1996, all with first class honors in electrical engineering.

As a Ph.D. student, he received a scholarship from the DAAD (German Academic Exchange Service) from 1993 to 1996, and he was with the High Voltage Institute of RWTH Aachen, Aachen, Germany. He held an Assistant Professor position at AUT from 1997 to 2003, was an Associate Professor from 2004 to 2007, and has been a Professor since 2007. He is the author of about 950 journal and conference papers. His teaching and research interests include smart grids, microgrids, FACTS and HVDC systems, and monitoring of power transformers.

Prof. Gharehpetian is a member of the Power Engineering Group of AUT, which was selected as a Center of Excellence on Power Systems in Iran in 2001. He was selected by the Ministry of Higher Education as a Distinguished Professor of Iran and by the Iranian Association of Electrical and Electronics Engineers (IAEEE) as a Distinguished Researcher of Iran and was awarded the National Prize in 2008 and 2010. Based on the ISI Web of Science database (2005–2015), he is among the world's top 1% elite scientists according to the Essential Science Indicators ranking system. He is a Distinguished Member of the IAEEE, and a member of the Central Board of the IAEEE. Since 2004, he has been the Editor-in-Chief of the *Journal of the IAEEE*.